What is claim d is:

1. A capacitor of an integrated circuit device comprising:

a first insulation layer formed on a semiconductor substrate, the first insulation layer having a buried contact hole formed therein;

a buried contact plug filling a portion of the buried contact hole to a predetermined height;

a diffusion barrier spacer formed on the buried contact plug and on an inner side surface of an upper portion of the buried contact hole above the buried contact plug;

a second insulation layer formed on the first insulation layer, the second insulation layer having a through hole with a diameter that is larger than that of the buried contact hole, wherein the diffusion barrier spacer and a top surface portion of the contact plug are exposed through the through hole;

a barrier layer formed on a bottom portion and a side surface of the through hole;

a lower electrode formed on the barrier layer;

a dielectric layer formed on the lower electrode and an upper surface of the second insulation layer; and

an upper electrode formed on the dielectric layer.

2. A capacitor of an integrated circuit device as claimed in claim 1, wherein the barrier layer is uniformly formed to a predetermined thickness.

3. A capacitor of an integrated circuit device as claimed in claim 1, wherein the lower electrode is uniformly formed to a predetermined thickness.

4. A capacitor of an integrated circuit device as claimed in claim 1, wherein the dielectric layer is uniformly formed to a predetermined thickness.

5. A capacitor of an integrated circuit device as claimed in claim 1, wherein the upper electrode is uniformly formed to a predetermined thickness.

6. A capacitor of an integrated circuit device as claimed in claim 1, wherein the diffusion barrier spacer is comprised of Al_2O_3.

7. A capacitor of an integrated circuit device as claimed in claim 1, wherein the diffusion barrier spacer has a thickness of about 50 Å to 500 Å.

8. A capacitor of an integrated circuit device as claimed in claim 1, wherein the upper electrode is comprised of any one selected from the group consisting of Pt, Ru, Ir, RuOx, IrOx and a mixture thereof.

9. A capacitor of an integrated circuit device as claimed in claim 1, wherein the lower electrode is comprised of any one selected from the group consisting of Pt, Ru, Ir, RuOx, IrOx and a mixture thereof.

10. A capacitor of an integrated circuit device as claimed in claim 1, wherein the barrier layer is comprised of TiN, TiSiN or TaN.

11. A capacitor of an integrated circuit device as claimed in claim 1, wherein the dielectric layer is comprised of at least one selected from the group consisting of Ta_2O_5, TaOxNy, Al_2O_3, (Ba, Sr)TiO_3[BST], $SrTiO_3$[ST], Pb(Zi, Ti)O_3[PLZT], SBT and a mixture thereof.

12. A capacitor of an integrated circuit device as claimed in claim 1, further comprising an etching stop layer disposed between the first insulation layer and the second insulation layer.

13. A capacitor of an integrated circuit device as claimed in claim 12, wherein the etching stop layer is a nitride layer.

14. A capacitor of an integrated circuit device as claimed in claim 1, wherein an upper surface of the first insulation layer is planarized by a chemical mechanical polishing (CMP) process.

15. A capacitor of an integrated circuit device as claimed in claim 1, further comprising a diffusion barrier layer between the first insulation layer and the second insulation layer.

16. A capacitor of an integrated circuit device as claimed in claim 15, wherein the diffusion barrier layer is comprised of Al_2O_3.

17. A capacitor of an integrated circuit device as claimed in claim 15, wherein the diffusion barrier layer has a thickness of about 50 Å to 500 Å.

18. A method of manufacturing a capacitor of an integrated circuit device comprising:

forming a first insulation layer on a semiconductor substrate;

forming a buried contact hole in the first insulation layer;

forming a buried contact plug in the buried contact hole to partially fill the buried contact hole;

forming a diffusion barrier spacer on the contact plug and on an inner side surface of an upper portion of the buried contact hole above the buried contact plug;

subsequently forming an etching stop layer and a second insulation layer on the semiconductor substrate including the buried contact hole and the buried contact plug;

partially etching the second insulation layer and the etching stop layer to form a through hole to expose a top surface of the buried contact plug and the diffusion barrier spacer, the through hole having a diameter that is larger than of the buried contact hole;

forming a barrier layer on a bottom and a side surface of the through hole along a surface profile of the through hole;

forming a lower electrode on the barrier layer;

forming a dielectric layer on the lower electrode and an upper surface of the second insulation layer;

heat treating the dielectric layer in an oxidation atmosphere to crystallize the dielectric layer; and

forming an upper electrode on the dielectric layer.

19. A capacitor of an integrated circuit device as claimed in claim 18, wherein the barrier layer is uniformly formed to a predetermined thickness.

20. A capacitor of an integrated circuit device as claimed in claim 18, wherein the lower electrode is uniformly formed to a predetermined thickness.

21. A capacitor of an integrated circuit device as claimed in claim 18, wherein the dielectric layer is uniformly formed to a predetermined thickness.

22. A capacitor of an integrated circuit device as claimed in claim 18, wherein the upper electrode is uniformly formed to a predetermined thickness.

23. The method of manufacturing a capacitor of an integrated circuit device as claimed in claim 18, wherein the diffusion barrier spacer is comprised of Al_2O_3.

24. A method of manufacturing a capacitor of an integrated circuit device comprising:

forming a first insulation layer on a semiconductor substrate;

forming a buried contact hole in the first insulation layer;

forming a buried contact plug in the buried contact hole to fill a portion of the buried contact hole;

forming a diffusion barrier layer on the first insulation layer, on the buried contact plug and on an inner side surface of an upper portion of the buried contact hole above the buried contact plug, the diffusion barrier layer having a uniform thickness along a surface profile of the buried contact hole;

forming a second insulation layer on the diffusion barrier layer;

etching the second insulation layer and the diffusion barrier layer to form a through hole to expose a top surface of the buried contact plug and a diffusion barrier spacer on an inner side surface of the upper portion of the buried contact hole, the through hole having a diameter that is larger than that of the buried contact hole;

forming a barrier layer on a bottom and a side surface of the through hole along a surface profile of the through hole;

forming a lower electrode on the barrier layer;

forming a dielectric layer on the lower electrode and an upper surface of the second insulation layer;

heat treating the dielectric layer in an oxygen atmosphere to crystallize the dielectric layer; and

forming an upper electrode on the dielectric layer.

25. A capacitor of an integrated circuit device as claimed in claim 24, wherein the barrier layer is uniformly formed to a predetermined thickness.

26. A capacitor of an integrated circuit device as claimed in claim 24, wherein the lower electrode is uniformly formed to a predetermined thickness.

27. A capacitor of an integrated circuit device as claimed in claim 24, wherein the dielectric layer is uniformly formed to a predetermined thickness.

28. A capacitor of an integrated circuit device as claimed in claim 24, wherein the upper electrode is uniformly formed to a predetermined thickness.

29. The method of manufacturing a capacitor of an integrated circuit device as claimed in claim 24, wherein the diffusion barrier layer is comprised of Al_2O_3.

30. The method of manufacturing a capacitor of an integrated circuit device as claimed in claim 24, wherein the barrier layer and the lower electrode are polished by a chemical mechanical polishing (CMP) process so that the barrier layer and the lower electrode are divided into a node unit.

31. A capacitor of an integrated circuit device comprising:

an insulation layer which is formed on a semiconductor substrate and has a buried contact hole formed therein;

a buried contact plug filling a portion of the buried contact hole to a predetermined height;

a diffusion barrier spacer which is formed on the buried contact plug and on an inner side surface of an upper portion of the buried contact hole above the buried contact plug;

a barrier layer uniformly formed in the buried contact hole and around the buried contact hole on the insulation layer along a surface profile of the buried contact hole;

a lower electrode uniformly formed on the barrier layer;

a dielectric layer uniformly formed on the lower electrode and the insulation layer; and

an upper electrode uniformly formed on the dielectric layer.

32. A capacitor of an integrated circuit device as claimed in claim 31, wherein the barrier layer is uniformly formed to a predetermined thickness.

33. A capacitor of an integrated circuit device as claimed in claim 31, wherein the lower electrode is uniformly formed to a predetermined thickness.

34. A capacitor of an integrated circuit device as claimed in claim 31, wherein the dielectric layer is uniformly formed to a predetermined thickness.

35. A capacitor of an integrated circuit device as claimed in claim 31, wherein the upper electrode is uniformly formed to a predetermined thickness.

36. The capacitor of an integrated circuit device as claimed in claim 31, wherein the diffusion barrier spacer is comprised of Al_2O_3.

37. The capacitor of an integrated circuit device as claimed in claim 31 wherein the diffusion barrier spacer has a thickness of about 50 Å to 500 Å.

38. A method of manufacturing a capacitor of an integrated circuit device comprising:

forming an insulation layer on a semiconductor substrate;

forming a buried contact hole in the insulation layer;

forming a buried contact plug in the buried contact hole to fill a portion of the buried contact hole;

forming a diffusion barrier spacer on the contact plug and on an inner side surface of an upper portion of the buried contact hole;

forming a barrier layer in the buried contact hole and around the buried contact hole on the insulation layer along a surface profile of the buried contact plug;

forming a lower electrode on the barrier layer;

forming a dielectric layer on the lower electrode and the insulation layer; and

forming an upper electrode on the dielectric layer.

39. The method of manufacturing a capacitor of an integrated circuit device as claimed in claim 38, wherein the diffusion barrier spacer is comprised of Al_2O_3.

40. The method of manufacturing a capacitor of an integrated circuit device as claimed in claim 38, wherein the barrier layer and the lower electrode are etched using the same etching mask so that the barrier layer and the lower electrode are divided into a node unit.

41. A capacitor of an integrated circuit device as claimed in claim 38, wherein the barrier layer is uniformly formed to a predetermined thickness.

42. A capacitor of an integrated circuit device as claimed in claim 38, wherein the lower electrode is uniformly formed to a predetermined thickness.

43. A capacitor of an integrated circuit device as claimed in claim 38, wherein the dielectric layer is uniformly formed to a predetermined thickness.

44. A capacitor of an integrated circuit device as claimed in claim 38, wherein the upper electrode is uniformly formed to a predetermined thickness.